Numerical Simulation of Microstrip Resonators and Filters Using the ADI–FDTD Method

Takefumi Namiki, *Member, IEEE*, and Koichi Ito, *Member, IEEE*

***Abstract*—In this paper, we derived the characteristics of typical and practical microstrip components such as microstrip linear resonators and microstrip low-pass filters using the alternating-direction-implicit–finite-difference-time-domain (ADI–FDTD) method to examine the calculation accuracy and efficiency of the method. The resonators and the filters included very narrow gaps and strips, respectively. In this case, very fine cells must be applied there for the finite-difference time-domian (FDTD) modeling. In the conventional FDTD method, fine cells cause a reduction of the time-step size because of the Courant–Friedrich–Levy (CFL) stability condition, which results in an increase in calculation time. In the ADI–FDTD method, on the other hand, a larger time-step size than the CFL stability condition limitation could be set. We compared the results of the ADI–FDTD method for various time-step sizes with the results of the conventional FDTD method and measured data.**

***Index Terms*—ADI–FDTD method, CFL stability condition, FDTD method, microstrip filter, microstrip resonator.**

I. Introduction

We previously proposed the alternating-direction-implicit–finite-difference-time-domain (ADI–FDTD) method for solving two-dimensional Maxwell's equations [1] and extended to three dimensions [2]–[4]. We showed that the algorithm of the method is unconditionally stable and free from the Courant–Friedrich–Levy (CFL) stability condition restraint [5]. Soon after having published our work, Zheng *et al.* reported the same approach [6] and theoretically proved the stability of the scheme in three dimensions [7]. Since the limitation on the maximum time-step size in the ADI–FDTD method is no longer dependent on the CFL stability condition, the maximum time-step size is limited by numerical errors that depend on what kinds of problems or models are calculated. In this paper, we derived the characteristics of typical and practical microstrip components such as microstrip linear resonators and microstrip low-pass filters using the ADI–FDTD method in order to examine the calculation accuracy and efficiency of the method. The resonators and filters included very narrow gaps and strips, respectively. In this case, very fine cells must be applied for the finite-difference time-domain (FDTD) modeling. In the conventional FDTD method, fine cells cause an increase in the total number of cells in the computational domain and a decrease in the time-step size because of the CFL stability condition, thereby increasing the required CPU time for these calculations. The former can be prevented by using nonuniform cells, but the latter cannot because the maximum time-step size is determined by the minimum cell size in the computational domain. On the other hand, a time-step size greater than the CFL stability condition limitation can be set when the ADI–FDTD method is used. We performed numerical simulations using the ADI–FDTD method to calculate the characteristics of the components for various time-step sizes and compared the results of the method with those of the conventional FDTD method and measured data in terms of accuracy and efficiency. All simulations in this paper were performed on an Ultra SPARCII 360-MHz workstation.

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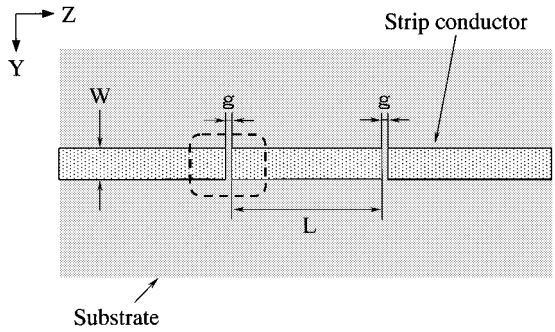


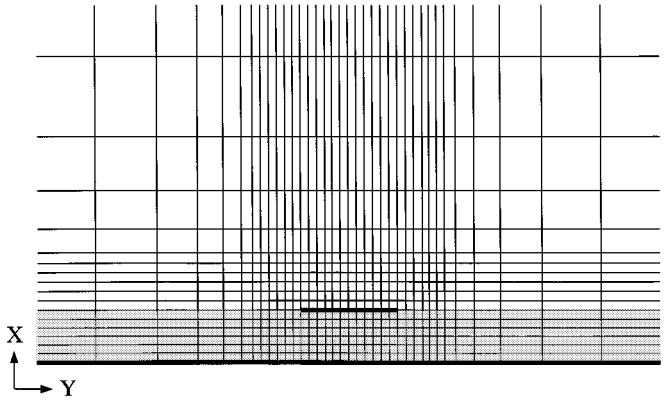
Fig. 1. Microstrip linear resonator (horizontal plane). The substrate was 810-μm thick with relative permittivity of 3.25. $W = 1.842$ mm, $L = 22$ mm, and $g = 80$ μm in Example 1. $W = 1.842$ mm, $L = 26.4$ mm, and $g = 20$ μm in Example 2. Spatial modeling in the xy-plane is shown in Fig. 2(a) and spatial modeling in the yz-plane of the region enclosed by the dashed line is shown in Fig. 2(b).

II. Microstrip Linear Resonator (Example 1)

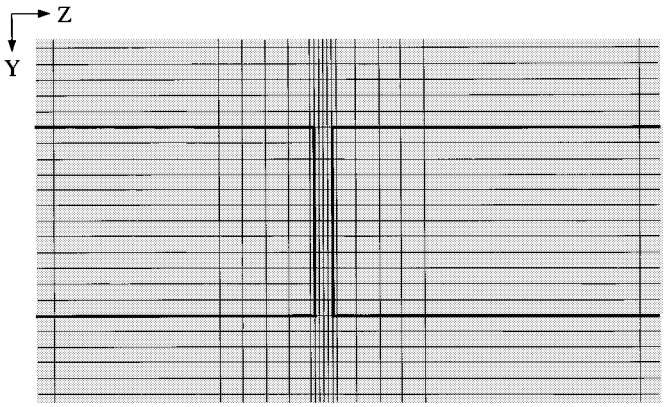
A. Structure and Modeling

Fig. 1 shows the horizontal structure of the microstrip linear resonator. Example 1 is characterized as follows. The substrate was 810-μm thick with relative permittivity of 3.25. The width and thickness of the strip was 1.842 mm and 18 μm, respectively, thereby rendering the thickness negligible for numerical modeling. There were two gaps with widths of 80 μm. The length of the internal strip was 22 mm.

We used nonuniform cells in order to treat the narrow gaps and long microstrip lines. The spatial modeling is shown in detail in Fig. 2. The substrate region was divided into six cells in the x-direction and the strip region was divided into 12 cells in the y-direction. An 80-μm-wide gap region was divided into four cells in the z-direction, in which the minimum cells, which were $153.5 \times 135 \times 20$ μm^3, were placed. The CFL stability



(a)



(b)

Fig. 2. Spatial modeling of the microstrip linear resonator. (a) Vertical plane. (b) Horizontal plane.

condition of this model was derived from the minimum cells and was $dt \leq 65.4059$ fs. The total number of cells was $22 \times 44 \times 78 = 75504$. Perfect electric conductor (PEC) boundary conditions were applied at the strips and at the ground plane. Mur's first-order absorbing boundary conditions (ABCs) [8] were applied on all outer surfaces, except the bottom ground plane. A Gaussian pulse was excited at one terminal and the output voltage was observed at the other terminal. By applying a Fourier transformation to the incident and output pulses, the insertion loss of the resonator could be calculated.

The time-step size for the conventional FDTD method was set so as to satisfy the CFL stability condition, and the time-step size for the ADI–FDTD method was set to 5, 10, or 20 times as large as the previous size. A physical time of each simulation, which was a product of the time-step size and the number of time–loop iterations, was required about 12 ns for the oscillation of the output pulse to converge. As a matter of course, the spatial modeling was the same for all these time-stepping models.

B. Numerical Results

The calculated and measured insertion losses of the resonator are shown in Fig. 3. The time-step size and required CPU time for each calculation are shown in Table I. The required memory size for the ADI–FDTD method was about 1.9 times as large as that for the conventional FDTD method because of the necessity of using extra electromagnetic component and coefficient array storage, which was common to all other examples.

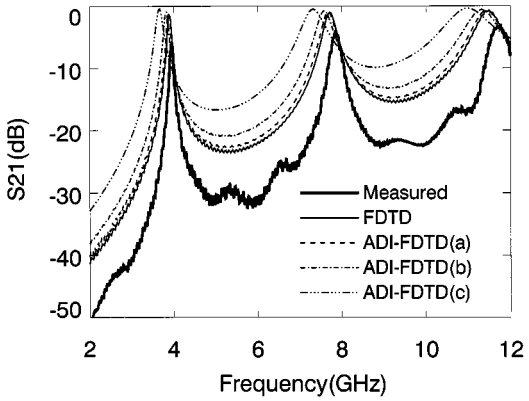


Fig. 3. Insertion loss of the microstrip linear resonator (Example 1).

TABLE I
TIME-STEP SIZE AND REQUIRED CPU TIME FOR THE SIMULTAION OF THE MICROSTRIP LINEAR RESONATOR (EXAMPLE 1)

	Time-step size		CPU time	
	fs	ratio	min	ratio
FDTD	65.0	1.0	68.1	1.00
ADI-FDTD (a)	325.0	5.0	72.7	1.07
ADI-FDTD (b)	650.0	10.0	33.4	0.49
ADI-FDTD (c)	1300.0	20.0	16.8	0.25

The calculated insertion loss of the FDTD is quite similar to the measured data although the level of the FDTD is a little high and its response is shifted downward slightly in terms of frequency. Comparing the results of the ADI–FDTD method with those of the conventional FDTD method, we can see that there are differences depending on the time-step size. However, the difference between the ADI–FDTD(a) and the FDTD can be ignored because such a small degree of difference can easily be a result of different spatial modeling. The resonant frequencies extracted from the insertion losses are shown in Table II, which also shows the relative errors of the calculated results with respect to the measured data. It can be seen, quantitatively, that the increase in time-step size resulted in a reduction of the resonant frequency.

As mentioned above, the tradeoff resulting from an increase in time-step size, which effects a reduction in CPU time, is an increase in numerical errors. Example 1 is a sample indicating that the ADI–FDTD method can be as accurate and efficient as the conventional FDTD method.

The ADI–FDTD method will have an advantage over the conventional FDTD method if a similar model includes smaller minimum cells in the computational domain, as is presented in Section III.

III. MICROSTRIP LINEAR RESONATOR (EXAMPLE 2)

A. Structure and Modeling

The microstrip linear resonator of Example 2 was the same as Example 1, except the width of the two gaps was 20 μm and the length of the internal strip was 26.4 mm.

TABLE II
RESONANT FREQUENCIES OF THE MICROSTRIP LINEAR RESONATOR (EXAMPLE 1)

	First mode		Second mode		Third mode	
	Resonant frequency	Relative error	Resonant frequency	Relative error	Resonant frequency	Relative error
Measured	3.95 GHz	——	7.85 GHz	——	11.76 GHz	——
FDTD	3.90 GHz	1.3%	7.72 GHz	1.7%	11.48 GHz	2.4%
ADI-FDTD (a)	3.87 GHz	2.0%	7.68 GHz	2.2%	11.46 GHz	2.6%
ADI-FDTD (b)	3.83 GHz	3.0%	7.58 GHz	3.4%	11.31 GHz	3.8%
ADI-FDTD (c)	3.66 GHz	7.3%	7.32 GHz	6.8%	10.99 GHz	6.5%

We used nonuniform cells again, and the spatial modeling details were quite similar to that of Example 1. The 20-μm-wide gap region was divided into four cells in the z-direction, in which the minimum cells, which were $153.5 \times 135 \times 5$ μm^3, were placed. The CFL stability condition of this model was $dt \leq 16.6464$ fs. The boundary conditions, such as the PEC, ABC, and the excitation condition, were applied in the same way as that of Example 1.

The time-step size for the conventional FDTD method was set so as to satisfy the CFL stability condition, and the time-step size for the ADI–FDTD method was set to 20 times as large as the previous size. A physical time of each simulation was set to 8 ns.

B. Numerical Results

The calculated insertion losses of the resonator are shown in Fig. 4, and it can be seen that the results of the FDTD are quite similar to the results of the ADI–FDTD. The time-step size and the required CPU time for each calculation are shown in Table III. The resonant frequencies extracted from the insertion losses are shown in Table IV. It can be seen that the CPU time of the ADI–FDTD could be reduced to about 26% of the FDTD while maintaining about the same level of accuracy.

The results of Examples 1 and 2 suggest that the ADI–FDTD method is more efficient than the conventional FDTD if the gap of the resonator is even narrower.

IV. MICROSTRIP LOW-PASS FILTER (EXAMPLE 3)

A. Structure and Modeling

Fig. 5 shows the horizontal structure of the microstrip low-pass filter introduced by Willke and Gearhart [9]. The substrate was 420-μm thick with relative permittivity of 3.81. The filter was composed of several parts of microstrip lines having different widths and lengths. L_1, L_2, L_3, and L_4 were 1.8, 1.929, 2.732, and 2.061 mm in length, respectively. Example 3 model is characterized as follows. W_a, W_b, and W_c were 100, 850, and 1500 μm in width, respectively. The thickness of the metal strip was 220 μm, thereby rendering it important for the numerical modeling.

We used nonuniform cells in order to treat both the narrow and wide strips. The spatial modeling is shown in detail in Fig. 6. The substrate region was divided into four cells and the strip region was also divided into four cells in the x-direction. The 100-μm-wide narrow strip region was divided into four cells in the y-direction, in which the minimum cells, which were $55 \times 25 \times 170.7$ μm^3, were placed. The CFL stability condition of this model was $dt \leq 75.1984$ fs. The total number of cells

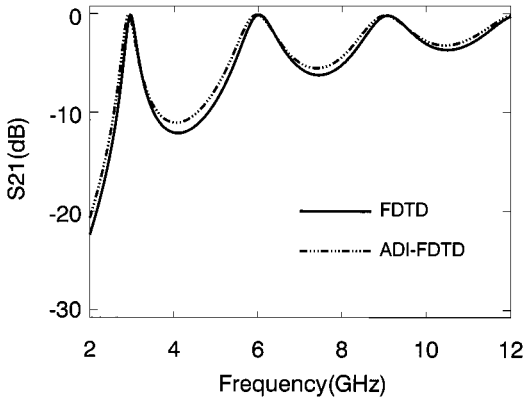


Fig. 4. Insertion loss of the microstrip linear resonator (Example 2).

TABLE III
TIME-STEP SIZE AND REQUIRED CPU TIME FOR THE SIMULTAION OF THE MICROSTRIP LINEAR RESONATOR (EXAMPLE 2)

	Time-step size		CPU time	
	fs	ratio	min	ratio
FDTD	16.64	1.0	175.2	1.00
ADI-FDTD	332.80	20.0	46.1	0.26

TABLE IV
RESONANT FREQUENCIES OF THE MICROSTRIP LINEAR RESONATOR (EXAMPLE 2)

	First mode	Second mode	Third mode
FDTD	2.96 GHz	6.03 GHz	9.08 GHz
ADI-FDTD	2.93 GHz	5.96 GHz	9.05 GHz

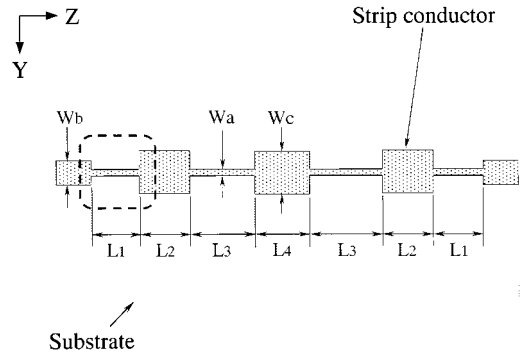


Fig. 5. Microstrip low-pass filter (horizontal plane). The substrate was 420-μm thick with relative permittivity of 3.81. L_1, L_2, L_3, and L_4 were 1.8, 1.929, 2.732, and 2.061 mm in length, respectively. Example 3 was characterized as follows. W_a, W_b, and W_c were 100, 850, and 1500 μm in width, respectively. The metal strip was 220-μm thick. Example 4 was characterized as follows. W_a, W_b, and W_c were 20, 850, and 850 μm in width, respectively. The metal strip was 20-μm thick. Spatial modeling in the xy-plane is shown in Fig. 6(a) and spatial modeling in the yz-plane of the region enclosed by the dashed line is shown in Fig. 6(b).

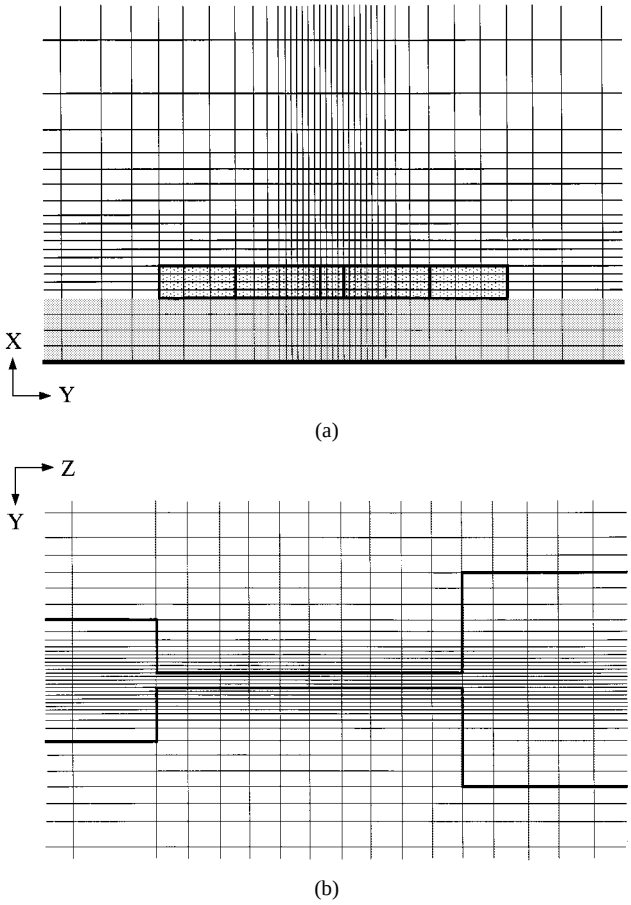


Fig. 6. Spatial modeling of the microstrip low-pass filter. (a) Vertical plane. (b) Horizontal plane.

was $23 \times 42 \times 122 = 117852$. PEC boundary conditions were applied at all strip surfaces including the ground plane. Mur's first-order ABC was applied on all outer surfaces, except the bottom ground plane. A partial-Gaussian pulse was excited at one terminal and the output voltage was observed at the other terminal. We then calculated the insertion loss of the filter.

The time-step size for the conventional FDTD method was set so as to satisfy the CFL stability condition, and the time-step size for the ADI–FDTD method was set to 5, 10, or 20 times as large as the previous size. A physical time of each simulation was set to about 2 ns.

B. Numerical Results

The calculated insertion losses of the filter are shown in Fig. 7, and includes measured data (by Willke and Gearhart [9]). The time-step size and the required CPU time for each calculation are shown in Table V. The results of the FDTD are on the whole similar to the measured data although its response is shifted downward in terms of frequency. Comparing the calculated results of the ADI–FDTD method with those of the conventional FDTD method, it can be seen that the increase in the time-step size shifted the response downward in terms of frequency. The -3- and -20-dB response frequencies of the filter extracted from the insertion losses are shown in Table VI, which includes the relative errors of the calculated results with respect to the measured data.

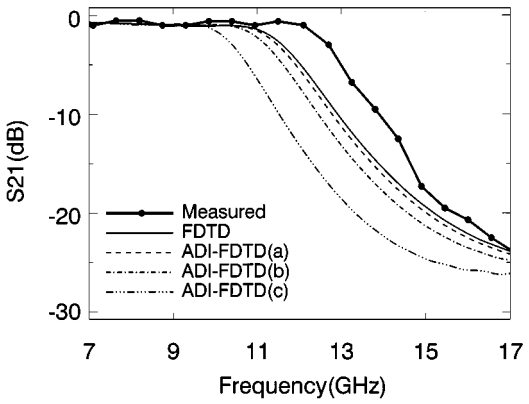


Fig. 7. Insertion loss of the microstrip low-pass filter (Example 3).

TABLE V
TIME-STEP SIZE AND REQUIRED CPU TIME FOR THE SIMULTAION OF THE MICROSTRIP LOW-PASS FILTER (EXAMPLE 3)

	Time-step size		CPU time	
	fs	ratio	min	ratio
FDTD	75.1	1.0	18.6	1.00
ADI-FDTD (a)	375.5	5.0	17.0	0.91
ADI-FDTD (b)	751.0	10.0	8.5	0.46
ADI-FDTD (c)	1502.0	20.0	4.3	0.23

TABLE VI
FREQUENCY OF -3- AND -20-dB RESPONSES OF THE MICROSTRIP LOW-PASS FILTER (EXAMPLE 3)

	-3dB response		-20dB response	
	Frequency	Relative error	Frequency	Relative error
Measured	12.70 GHz	——	15.80 GHz	——
FDTD	11.60 GHz	8.7 %	15.20 GHz	3.8 %
ADI-FDTD (a)	11.49 GHz	9.5 %	15.04 GHz	4.8 %
ADI-FDTD (b)	11.22 GHz	11.7 %	14.58 GHz	7.7 %
ADI-FDTD (c)	10.41 GHz	18.0 %	13.33 GHz	15.6 %

As in the case of the previous microstrip resonator, the tradeoff resulting from an increase in time-step size is an increase in numerical errors. Example 3 is also a sample indicating that the ADI–FDTD method can be as accurate and efficient as the conventional FDTD method.

In order to show the advantage of using the ADI–FDTD method, another example, which is a similar model that includes smaller minimum cells in the computational domain, is presented in Section V.

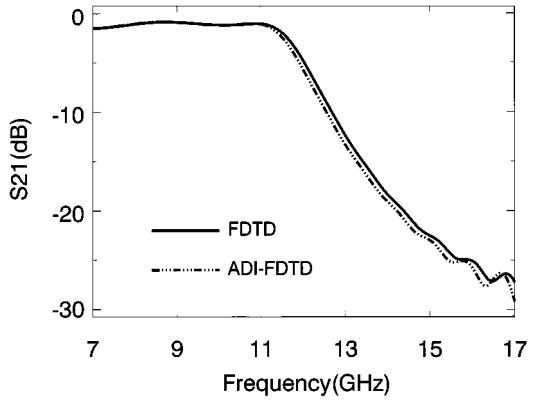


Fig. 8. Insertion loss of the microstrip low-pass filter (Example 4).

TABLE VII
TIME-STEP SIZE AND REQUIRED CPU TIME FOR THE SIMULTAION OF THE MICROSTRIP LOW-PASS FILTER (EXAMPLE 4)

	Time-step size		CPU time	
	fs	ratio	min	ratio
FDTD	11.78	1.0	127.0	1.00
ADI-FDTD	117.80	10.0	52.2	0.41

TABLE VIII
FREQUENCY OF −3- AND −20-dB RESPONSES OF THE MICROSTRIP LOW-PASS FILTER (EXAMPLE 4)

	-3dB response	-20dB response
FDTD	11.72 GHz	14.38 GHz
ADI-FDTD	11.61 GHz	14.22 GHz

V. MICROSTRIP LOW-PASS FILTER (EXAMPLE 4)

A. Structure, Spatial Modeling, and Time-Stepping Modeling

The microstrip filter of Example 4 was the same as Example 3, except the width and thickness of the metal strip were different. W_a, W_b, and W_c were 20, 850, and 850 μm in width, respectively. The metal strip was 20-μm thick. The narrow strip region was divided into four cells, both in the x- and y-directions. The minimum cells placed there were $5 \times 5 \times 170.7$ μm^3. The CFL stability condition of this model was $dt \leq 11.7826$ fs. The simulation was carried out in the same way as in Example 3.

The time-step size for the conventional FDTD method was set so as to satisfy the CFL stability condition, and the time-step size for the ADI–FDTD method was set to ten times as large as the previous size.

B. Numerical Results

The calculated insertion losses of the filter are shown in Fig. 8. The time-step size and the required CPU time for each calculation are shown in Table VII. The −3 and −20–dB responses frequencies of the filter are shown in Table VIII. It can be seen that the results of the ADI–FDTD are quite similar to the results of the FDTD, and the CPU time of the ADI–FDTD can be reduced to about 41% of the FDTD while maintaining about the same level of accuracy.

The results of Examples 3 and 4 suggest that the ADI–FDTD method is more efficient than the conventional FDTD if the strip of the low-pass filter is even narrower.

VI. CONCLUSION

In this paper, numerical simulations of typical and practical microstrip components, such as microstrip linear resonators and microstrip low-pass filters, using the ADI–FDTD method have been presented. The results of the simulations are compared with those of the conventional FDTD method and measured data in terms of accuracy and efficiency.

We reconfirmed that the ADI–FDTD method guarantees a stable calculation in any time-step size and that a large time-step size reduces both the number of time–loop iterations and the required CPU time for the calculation. However, we also found that a large time-step size causes numerical errors. In other words, the tradeoff resulting from an increase in time-step size is an increase in numerical errors. Since the increase in time-step size shifted the response downward in terms of frequency, the numerical errors are most likely caused by numerical dispersions [10].

In the microstrip components shown here, the required CPU time of the ADI–FDTD method can be equivalent to or shorter than that of the conventional FDTD method while maintaining about the same level of accuracy. If the local minimum cells in the domain are smaller, the ADI–FDTD method will be more efficient.

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